

Remarks

The instant Office Action dated March 20, 2008 notes the following rejections: claims 1, 3, 5, 7-8 and 10 stand rejected under 35 U.S.C. § 103(a) over Chudzik (U.S. Patent No. 7,030,481) in view of Larson *et al.* (U.S. Patent No. 5,495,117); claims 2, 4 and 6 stand rejected under 35 U.S.C. § 103(a) over Chudzik and Larson and further in view of Kosaki *et al.* (U.S. Patent No. 6,268,619); and claim 9 stands rejected under 35 U.S.C. § 103(a) over Chudzik and Larson and further in view of Goldberger *et al.* (U.S. Patent No. 6,538,300).

Applicant respectfully traverses the § 103(a) rejection of claims 1, 3, 5, 7-8 and 10 because the cited portions of the Chudzik and Larson references do not correspond to the claimed invention which includes, for example, aspects directed to a layer of dielectric material, which is used as the dielectric of a vertical trench capacitor and also as insulation between a substrate and a vertical interconnect that extends through the substrate. The Examiner appears to be confusing Chudzik's teachings relating to separate dielectric layers that can be the same type of material with the claimed invention, which has a single dielectric layer that is both the dielectric of a vertical trench capacitor and insulation between a substrate and a vertical interconnect. *See, e.g.*, page 7:19 to page 8:3 of the instant Office Action. More specifically, the cited portions of the Chudzik reference do not teach that insulating material 220, which separates the conductive material 230 in via 210 from the substrate 200, is the same layer of dielectric material that is used as the dielectric film 3020 of the trench capacitor structures 3010. *See, e.g.*, Figure 3b and Col. 4:13-15. In other words, Chudzik does not teach that insulating material 220 and dielectric film 3020 are part of the same layer of dielectric material; Chudzik simply teaches that these two separate layers (220 and 3020) could be formed of the same type of dielectric material. Accordingly, the cited portions of Chudzik do not teach that the same layer of dielectric material is used as both the dielectric of a vertical trench capacitor and to provide insulation between a substrate and a vertical interconnect as in the claimed invention.

Moreover, Applicant submits that the cited portions of the Larson reference are essentially unrelated to the claimed invention because Larson does not teach that insulating layers (20, 26, and 36) provide insulation between a substrate and a vertical interconnect that extends through the substrate or that these insulating layers form the dielectric of a vertical trench capacitor. The Examiner's erroneous assertion that Larson teaches that insulating

layers (20, 26, and 36) are used as insulation between a substrate and a vertical interconnect is directly contradicted by the cited portions of Larson which teach that these insulating layers (20, 26, and 36) are deposited over a transistor 10, which is fabricated on a substrate. *See, e.g.*, Figure 4F and Col. 3:46-57. Larson does not mention any vertical interconnect that extends through this substrate or that Larson's insulating layers (20, 26, and 36) are used as insulation between this substrate and some apparently nonexistent vertical interconnect. The cited portions of Larson also do not mention that these insulating layers (20, 26, and 36) are used as the dielectric in a vertical trench capacitor. Accordingly, the cited portions of Larson do not teach that insulating layers (20, 26, and 36) form the dielectric of a vertical trench capacitor or that these insulating layers provide insulation between a substrate and a vertical interconnect that extends through the substrate.

In view of the above, the cited combination of the Chudzik and Larson references does not correspond to the claimed invention. Accordingly, the § 103(a) rejection of claims 1, 3, 5, 7-8 and 10 is improper and Applicant requests that it be withdrawn.

Applicant further traverses the § 103(a) rejection of claim 3 because the cited portions of the Chudzik reference do teach that the vertical interconnect includes a plurality of parallel trenches that are each substantially filled with conductive material. The Examiner asserts that Chudzik's via 210 corresponds to the claimed vertical interconnect (*see, e.g.*, page 3 of the instant Office Action); however, Chudzik does not teach that via 210 includes a plurality of parallel trenches (*see, e.g.*, Figures 3b and 4a). The Examiner then improperly attempts to show correspondence to the plurality of parallel trenches by citing to another via 410' that is filled with conductive filler 430'. *See, e.g.*, Figure 4a and Col. 6:13-25. Thus, the cited portions of Chudzik teach a plurality of vias (*i.e.*, a plurality of vertical interconnects), instead of a vertical interconnect that includes a plurality of parallel trenches that are each substantially filled with conductive material as in the claimed invention. Accordingly, the § 103(a) rejection of claim 3 is improper and Applicant requests that it be withdrawn.

Applicant respectfully traverses the § 103(a) rejections of claims 2, 4, 6 and 9 (each of which is based on the Chudzik and Larson references) because the cited portions of these references do not correspond to the claimed invention as discussed above in relation to the § 103(a) rejection of claim 1. In at least this regard, the § 103(a) rejections of claims 2, 4, 6

and 9 are improper because these claims depend from claim 1. That is, if an independent claim is nonobvious under 35 U.S.C. § 103, then any claim depending therefrom is nonobvious. *See, In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). Accordingly, the § 103(a) rejections of claims 2, 4, 6 and 9 are improper and Applicant requests that they be withdrawn.

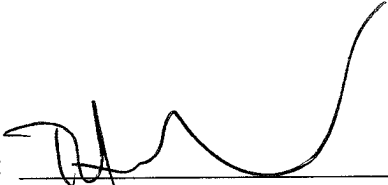
Applicant further traverses the § 103(a) rejection of claim 9 because the cited portions of the Goldberger reference do teach that a planar capacitor is present on the first side of the substrate. Specifically, the cited portions of Goldberger teach that the second plate of the capacitor is the substrate 102. *See, e.g.*, Figure 1 and Col. 3:19-24. Thus, Goldberger teaches that the substrate 102 forms part of the capacitor, instead of a planar capacitor that is on the first side of the substrate as claimed. Moreover, the Examiner erroneously asserts that Goldberger teaches that the dielectric material (*i.e.*, 104) of this capacitor is the same layer of dielectric material as some vertical trench capacitor. The cited portions of Goldberger do not mention any vertical trench capacitor, let alone that the same layer of dielectric material is used as the dielectric in both a planar capacitor and a vertical trench capacitor as claimed. Accordingly, the § 103(a) rejection of claim 9 is improper and Applicant requests that it be withdrawn.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063.

Please direct all correspondence to:

Corporate Patent Counsel
NXP Intellectual Property & Standards
1109 McKay Drive; Mail Stop SJ41
San Jose, CA 95131

CUSTOMER NO. 65913

By: 
Name: Robert J. Crawford
Reg. No.: 32,122
651-686-6633
(NXPS.351PA)